

國立中山大學 115 學年度 碩士班考試入學招生考試試題

科目名稱：計算機結構【資工系碩士班甲組、乙組】

—作答注意事項—

考試時間：100 分鐘

- 考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- 答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，請衡酌作答。
- 答案卡請以 2B 鉛筆劃記，不可使用修正液（帶）塗改，未使用 2B 鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，後果由考生自負。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶書籍、紙張（應考證不得做計算紙書寫）、具有通訊、記憶、傳輸或收發等功能之相關電子產品或其他有礙試場安寧、考試公平之各類器材入場。
- 試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。
- 試題採雙面列印，考生應注意試題頁數確實作答。
- 違規者依本校招生考試試場規則及違規處理辦法處理。

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科目名稱：計算機結構【資工系碩士班甲組、乙組】
※本科目依簡章規定「不可以」使用計算機(問答申論題)

題號：434001

共 4 頁 第 1 頁

Note: If any question is ambiguous or insufficiently specified, you are allowed to make reasonable assumptions. Please state and justify these assumptions clearly in your answer.

1. Short Conceptual Questions (20 points)

Q1.1 (7 points)

For several decades, processor performance improvements were largely achieved by increasing clock frequency. However, this approach eventually stopped being the primary driver of performance gains. Modern processors now rely heavily on techniques such as instruction-level parallelism, pipelining, speculative execution, and hierarchical memory systems.

Please explain why increasing clock frequency alone has become an ineffective and unsustainable method for improving processor performance. In your explanation:

1. (4 points) *Identify two fundamental physical or architectural constraints that limit the benefits of higher clock frequencies.*
2. (3 points) *Explain how each constraint directly motivates the architectural shift toward parallelism, prediction, and memory hierarchy.*

(Your answer should be based on core computer architecture principles rather than manufacturing or marketing considerations.)

Q1.2 (7 points)

A program executes on a processor with the following characteristics:

- Total instruction count: 2×10^9 instructions
- Instruction mix:
 - 50% arithmetic instructions, CPI = 1
 - 30% memory instructions, CPI = 5
 - 20% control instructions, CPI = 2
 - Processor clock frequency: 2 GHz

Please answer the following questions:

1. (3 points) *Compute the total CPU execution time of the program.*
2. (4 points) *The processor designer improves the memory system so that the CPI of memory instructions is reduced from 5 to 2. Compute the new execution time and the overall speedup.*

Q1.3 (6 points)

Many architectural optimizations are designed to “make the common case fast.” *Please explain what this principle means in practice and why violating it often leads to worse overall performance, even if rare cases become faster.*

2. Performance Analysis (20 points)

Q2.1 (10 points)

A program executes on a processor with the following characteristics:

- 35% of instructions are arithmetic instructions (CPI = 1)
- 45% are memory access instructions (CPI = 3)
- 20% are control instructions (CPI = 2)
- Clock cycle time = 0.4 ns

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共 4 頁 第 2 頁

The program executes 1 billion instructions.

Please calculate:

1. (5 points) *Average CPI*
2. (5 points) *Total CPU execution time*

Q2.2 (10 points)

An architect accelerates a floating-point unit so that floating-point instructions run five times faster. Originally, floating-point instructions account for 30% of total execution time. *Please use the fundamental performance laws to compute the maximum possible speedup of the entire program.*

3. Instruction Set Architecture (15 points)

Q3.1 (8 points)

A processor designer is considering adding complex instructions that directly operate on memory operands (thus potentially doing more work per instruction), which would reduce the number of instructions in programs but increase the complexity and latency of each instruction. *Considering architectural trade-off principles, please explain why modern instruction set architectures favor simple, RISC-style instructions even if this means executing more instructions to accomplish the same task.*

Q3.2 (7 points)

In modern 64-bit processors with fixed-length instructions and deep pipelines, conditional branch instructions almost always use PC-relative addressing, where the branch target is encoded as an offset from the current program counter, instead of using an absolute target address.

Consider the following design and system context:

- Programs may be loaded at different memory addresses due to dynamic linking, shared libraries, or address space layout randomization.
- Branch instructions are frequent and often target nearby instructions such as loop back-edges or conditional blocks.
- Deep pipelines require early branch target calculation to reduce control hazards.
- Instruction cache performance is sensitive to instruction size and code density.

Based on the above context, please answer the following two questions:

- (a) (4 points) *State two reasons at the instruction-set / system level why PC-relative addressing is preferred over absolute addressing.*
- (b) (3 points) *State one reason at the microarchitectural level why PC-relative addressing is especially beneficial for pipelined processors.*

Your answers should be concise and focus on architectural principles.

4. Computer Arithmetic (15 points)

Q4.1 (8 points)

A processor represents signed integers using 8-bit two's complement format. The most significant bit is used as the sign bit, and arithmetic is performed using standard two's complement rules. Consider the following design and usage context:

- All arithmetic operations are performed modulo 2^8 .
- Negation is implemented by bitwise inversion followed by adding 1.
- The same hardware is used for both signed and unsigned arithmetic.

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題號：434001
共 4 頁 第 3 頁

Please answer the following three questions

- (a) (3 points) determine the minimum and maximum integers that can be represented in this system.*
- (b) (3 points) Explain why the set of representable values is asymmetric, i.e., why there is one more negative value than positive value.*
- (c) (2 points) Identify which specific bit pattern causes this asymmetry and explain its role in two's complement arithmetic.*

Your answers should be concise and based on representation properties rather than examples alone.

Q4.2 (7 points)

A processor implements floating-point arithmetic using a fixed-precision binary floating-point format that rounds the result of every arithmetic operation to the nearest representable value. Consider the following scenario:

- You are given a very large array of floating-point numbers whose magnitudes vary widely.
- Two programs compute the sum of all elements in the array:
 - Program A sums the elements from left to right.
 - Program B sorts the elements by magnitude and sums from smallest to largest.
- Both programs use the same floating-point format and run on the same hardware.

Despite using identical arithmetic instructions, the two programs produce different results.

Please answer the following questions:

- (a) (4 points) State two fundamental properties of floating-point arithmetic that explain why the two programs may produce different sums.*
- (b) (3 points) Explain which summation order is expected to produce a more accurate result and why.*

Your answers should refer to representation and arithmetic properties of floating-point numbers, not implementation bugs or software errors.

5. Pipelining & Hazards (15 points)

Q5.1 (8 points)

Consider a 5-stage pipeline (IF, ID, EX, MEM, WB). A load instruction is immediately followed by an instruction that uses the loaded value (for example, LW R1, 0(R2) followed by ADD R3, R1, R4). *Please explain in detail: (1) (3 points) Why a data hazard occurs in this scenario, (2) (3 points) Why forwarding alone is insufficient to resolve it, and (3) (2 points) The minimum pipeline stall required (if any) to handle the hazard.*

Q5.2 (7 points)

Modern high-performance processors often use deep pipelines to increase clock frequency. However, deeper pipelines suffer higher penalties when branch predictions are incorrect. Assume the following simplified model:

- A branch is resolved at the end of the pipeline
- A mis-predicted branch causes all younger instructions in the pipeline to be flushed
- Branch prediction accuracy is fixed at 90%
- Each pipeline stage takes 1 cycle

Please answer the following two parts.

(a) Numerical Analysis (3 points)

For the following pipeline depths, please compute the branch misprediction penalty and the average misprediction cost per branch. Please draw a new table on your answer sheet for your answers.

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共 4 頁 第 4 頁

Pipeline Depth (stages)	Misprediction Penalty (cycles)	Average Cost per Branch (cycles)
5	?	?
10	?	?
20	?	?

(b) Based on your numerical results and graph, explain why deeper pipelines rely more heavily on accurate branch prediction, even when prediction accuracy does not change. (4 points)

6. Cache & Memory Hierarchy (15 points)

Q6.1 (8 points)

A system has a cache and memory with the following characteristics:

- Cache hit time = 1 cycle
- Cache miss rate = 2% (0.02)
- Miss penalty (time to fetch from lower-level memory on a miss) = 100 cycles

Please calculate the average memory access time (AMAT) for this system.

Q6.2 (7 points)

Increasing cache associativity reduces conflict misses but may degrade performance. Please explain why increasing associativity eventually hurts performance, using architectural cost reasoning.