

國立中山大學 111 學年度

碩士班暨碩士在職專班招生考試試題

科目名稱：計算機結構【資工系碩士班甲組、乙組】

— 作答注意事項 —

考試時間：100 分鐘

- 考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- 答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，請衡酌作答(不得另攜帶紙張)。
- 答案卡請以 2B 鉛筆劃記，不可使用修正液（帶）塗改，未使用 2B 鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，後果由考生自負。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶具有通訊、記憶或收發等功能或其他有礙試場安寧、考試公平之各類器材、物品（如鬧鈴、行動電話、電子字典等）入場。
- 試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。
- 試題採雙面列印，考生應注意試題頁數確實作答。
- 違規者依本校招生考試試場規則及違規處理辦法處理。

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科目名稱：計算機結構【資工系碩士班甲組、乙組】

題號：434001

※本科目依簡章規定「不可以」使用計算機(問答申論題)

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Problem 1: (10%)

1. (2%) Please explain why we need virtual memory and explain its pros and cons.
2. (2%) TLB is usually much smaller than the page table. Hence, fully associative is a good choice to design the TLB. Is it still a good choice to use fully associative if we enlarge the TLB size? Please explain your reasons.
3. (2%) The multi-level cache is usually applied in modern systems. Please determine what kind of strategy is proper for cache consistency in writing data.
4. (2%) Please explain the difference between the multi-word cache organization and set-associative organization and explain their pros and cons.
5. (2%) Please explain why the nonblocking cache can improve the cache bandwidth.

Problem 2: (30%)

You have to run a program, which requires 4GB of memory space. Unfortunately, your computer system only allocates 2GB DRAM to this program. Hence, applying the virtual memory technique is necessary, and we assume that the total page size is 4KB. Besides, you also implement the write-back consistency policy and the LRU replacement policy in this virtual memory technique.

1. (10%) How large is the involved page table at least?
2. (10%) We assume that the CPU in your system accesses the data in this program randomly (i.e., no data locality). At the quasi-stationary, please show the approximated page fault rate.
3. (10%) If we have a TLB in this system and the TLB miss rate is 75% at the quasi-stationary, how large is the involved TLB at least?

Problem 3: (25%)

Now, you have a 32-bit processor, including a cache with 16KB data. We assume that the write-back consistency policy and the LRU replacement policy are both implemented in this cache as well. Please analyze the different architecture designs below.

1. (5%) How many total bits are required if the direct-mapping strategy is involved, and the one-word block is considered?
2. (5%) How many total bits are required if the direct-mapping strategy is involved, and the four-word block is considered?
3. (5%) How many total bits are required if the two-way set-associative strategy is involved, and the four-word block is considered?
4. (5%) TLB is usually adopted in modern systems. If we use the 32-bit address to access the TLB with 10 entries and each page size is 4KB, how large is the involved TLB?
5. (5%) By following the previous question, how large is the involved page table?

Problem 4: (20%)

The clock cycle time of a given processor is 1ns. We assume only one level cache is installed in this system and every data can be found in the main memory. Besides, we know the miss penalty is 20 clock cycles; the average miss rate is 5%; the cache access time is one clock cycle. Today, we have a program, and 40% of codes can be executed parallelly.

1. (10%) Please find the average memory access time of this system.
2. (10%) How many cores do you have to use to double the performance of this system? Please explain your answer.

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Problem 5: (15%)

Figure 1 shows a 5-stage pipelined MIPS CPU to support a simple code in Figure 2. We need to spend one clock cycle to complete all tasks in each pipeline stage.

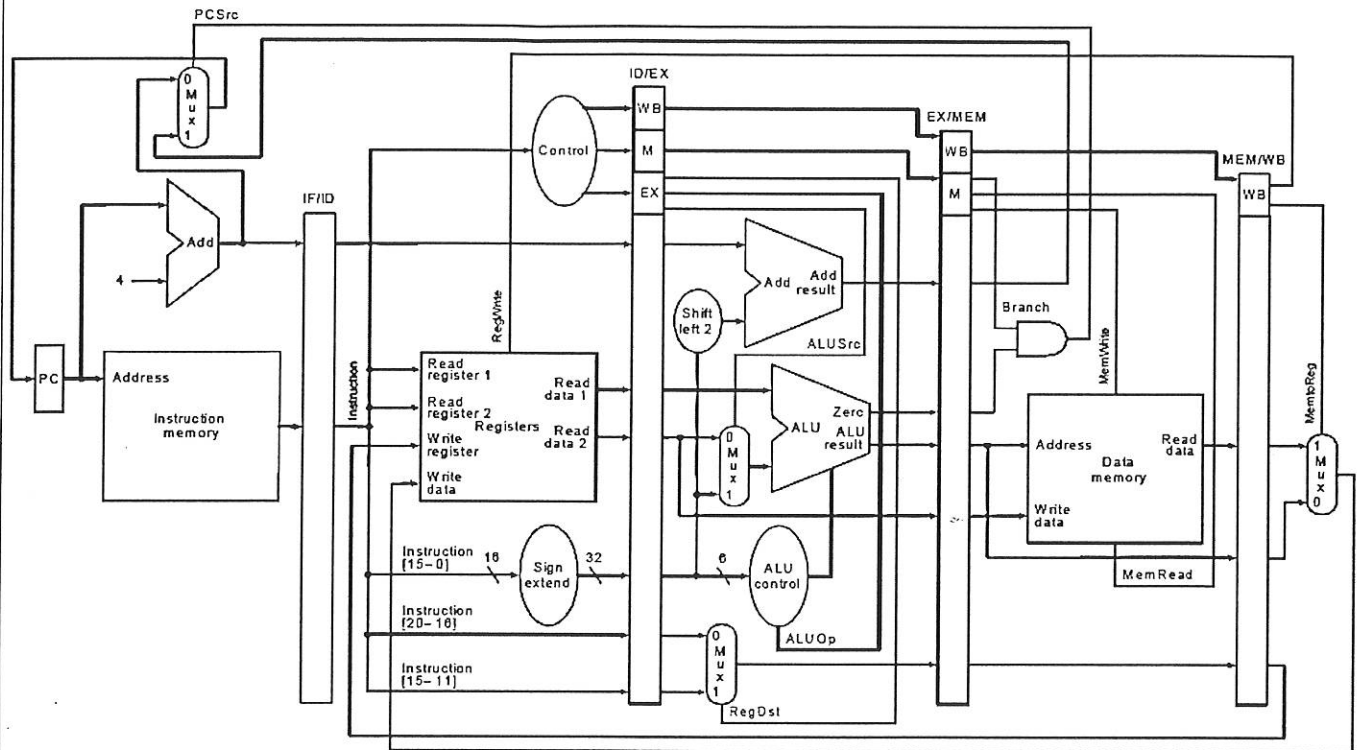


Figure 1

```
sub $2, $1, $3
and $12, $2, $5
or $13, $6, $2
add $14, $2, $2
sw $15, 100($2)
```

Figure 2

1. (5%) Do we need to stall this architecture in Figure 1 to run the code in Figure 2? If yes, please determine how many cycles we should stall and explain your reasons. If not, please describe your reason.
2. (5%) To support the code in Figure 2, please design a minimum viable product (MVP) of the ALU in Figure 1. You need to show the ALU architecture.
3. (5%) Is it possible to move the Adder from the third pipeline stage to the second pipeline stage? If yes, please explain your re-design strategy. If not, please describe your reason.