

# 國立中山大學 108 學年度 碩士暨碩士專班招生考試試題

科目名稱：計算機結構【資工系碩士班甲組、乙組】

## —作答注意事項—

考試時間：100 分鐘

- 考試開始響前不得翻閱試題，並不得書寫、劃記、作答。請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- 答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，不得另攜帶紙張，請衡酌作答。
- 答案卡請以 2B 鉛筆劃記，不可使用修正液（帶）塗改，未使用 2B 鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，其後果由考生自行負擔。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶具有通訊、記憶或收發等功能或其他有礙試場安寧、考試公平之各類器材、物品（如鬧鈴、行動電話、電子字典等）入場。
- 試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。
- 試題採雙面列印，考生應注意試題頁數確實作答。
- 違規者依本校招生考試試場規則及違規處理辦法處理。

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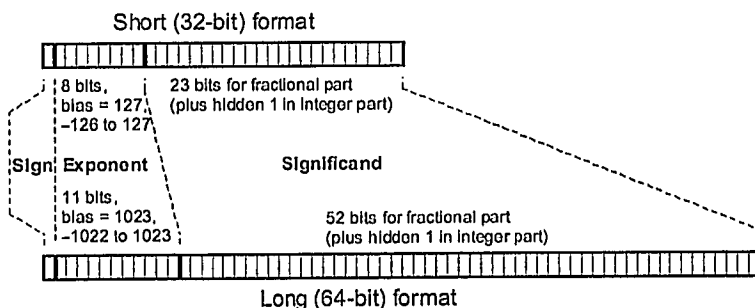
題號：434001

※本科目依簡章規定「不可以」使用計算機(問答申論題)

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## 1. (20%)

The following figure shows the IEEE 754 standard for floating-point representation of both single-precision (short) and double precision (long) formats to represent a regular floating number  $\pm 1.f \times 2^e$  where  $1.f$  is called significand and  $e$  is the exponent, and other special numbers.



|                          | single-precision (short)                                          | double precision (long)                                            |
|--------------------------|-------------------------------------------------------------------|--------------------------------------------------------------------|
| word width (bits)        | 32                                                                | 64                                                                 |
| significand bits         | 23+1 hidden                                                       | 52+1 hidden                                                        |
| exponent bits            | 8                                                                 | 11                                                                 |
| exponent bias            | 127                                                               | 1023                                                               |
| zero                     | $e + bias = 0, f = 0$                                             | $e + bias = 0, f = 0$                                              |
| subnormal                | $e + bias = 0, f \neq 0$ ,<br>represent $\pm 0.f \times 2^{-126}$ | $e + bias = 0, f \neq 0$ ,<br>represent $\pm 0.f \times 2^{-1022}$ |
| infinity ( $\pm\infty$ ) | $e + bias = 255, f = 0$                                           | $e + bias = 2047, f = 0$                                           |
| Not-a-Number (NaN)       | $e + bias = 255, f \neq 0$                                        | $e + bias = 2047, f \neq 0$                                        |
| ordinary number          | $e + bias \in [1, 254]$                                           | $e + bias \in [1, 2046]$                                           |

- 1.1 (2%) What is the binary representation of zero in the single-precision format? Express your answer using binary format similar to  $x\_xxxxxxxx\_xxxxxxxxxxxxxxxxxxxxxxxxxxxx$  where  $x$  is either 0 or 1.
- 1.2 (2%) What is the binary representation of the decimal value -0.5 in single precision format?
- 1.3 (2%) What is the maximum magnitude of ordinary numbers (i.e., excluding infinity, NaN, and subnormal numbers) in single precision floating-point representation? Express your answer in format of  $x.xx \cdots xx \times 2^e$  where  $x \in \{0, 1\}$  and  $e$  is the decimal value of the exponent.
- 1.4 (2%) What is the minimum magnitude of ordinary numbers (i.e., other than zero) in single precision floating-point representation? Express your answer in format of  $x.xx \cdots xx \times 2^e$  where  $x \in \{0, 1\}$  and  $e$  is the decimal value of the exponent.
- 1.5 (2%) What is the minimum magnitude of subnormal numbers in single precision floating-point representation? Express your answer in format of  $x.xx \cdots xx \times 2^e$  where  $x \in \{0, 1\}$  and  $e$  is the decimal value of the exponent.
- 1.6 (2%) What is the representable range of the single-precision floating-point numbers?
- 1.7 (2%) Is the distance between two neighboring single-precision floating-point numbers the same? Why?
- 1.8 (2%) For a 32-bit two's complement signed fixed-point representation with 16 integer bits and 16 fractional bits, is the distance between two neighboring numbers the same? Why?
- 1.9 (2%) Continued with the previous 32-bit signed fixed-point representation, what is the representable range of the 32-bit signed fixed-point format?
- 1.10 (2%) In general, addition of two 32-bit fixed-point numbers can be finished in one clock cycle. However, addition of two single-precision floating-point numbers usually takes more than one clock cycle. Why? Hint: explain using the operations involved in floating-point addition/subtraction.

試題請隨卷繳回

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## 2. (20%)

- 2.1 (5%) A processor is busy with computation 40% of the execution time, and is waiting for I/O access 60% of the execution time. If we replace the processor with a new one which is 10 times faster than the old processor, what is the overall speedup gained using the new processor assuming that the percentage of I/O access remains the same in both processors?
- 2.2 (5%) If you want to achieve a speedup of 80 for a computation task using 100 processors running concurrently, what fraction of the computation task can be sequential according to Amdahl's law?
- 2.3 (5%) For an application program running on a multi-processor system with 32 processors, it takes 200 ns to handle reference in a remote memory. Assume that this application program always has hits in the local memory except for remote memory access involving communication. Processors are stalled on a remote request, and the processor clock is 3.3 GHz. Assume that the base CPI (cycles per instruction) is 0.5 and all references hit in cache. How much faster is the multi-processor if there is no communication versus if 0.2% of instructions involve remote communication references? Hint: compute the new CPI first. The speedup is the ratio of the two CPI values.
- 2.4 (5%) Assume that 25% operations of a computation task are floating-point operations and average CPI (cycles per instruction) for floating-point operations and other operations are 4.0 and 1.33 respectively. Suppose that 2% of the floating-point operations in the task are floating-point division which has CPI = 20. Assume that the two design alternatives are to decrease the CPI of the floating-point division to 2 or the decrease the average CPI of all floating-point operations to 2.5. Compare these two design alternatives using processor performance equation. Which design choice is better? Why? Hint: compute the CPI values of different designs.

## 3. (20%)

A standard pipelined CPU contains five pipeline stages: instruction fetch (IF), instruction decode (ID), ALU execution (EX), memory access (MA), and result write-back (WB). Assume that the critical path delays of the five types of instruction operations IF, ID, EX, MA, WB are 20ns, 20ns, 50ns, 40ns, 30ns respectively.

- 3.1 (2%) What is the maximum working frequency of the above CPU?
- 3.2 (6%) Assume that a computation task contains only 100 instructions and there is no hazard for these instructions, what is the throughput of this task? What is the total latency of finishing executing this task? What is the average cycle per instruction (CPI) in this task?
- 3.3 (4%) If we want to reduce the pipelined stages from 5 to 4 by merging some of the five types of pipelined operations mentioned above, what is the best design if the speed performance is the first choice? And what is the maximum working frequency of the new design with four pipelined stages?
- 3.4 (4%) What is data hazard? Give an assembly language example to show one type of data hazard.
- 3.5 (4%) What is super-pipeline? What are the advantages and disadvantages of super-pipeline design?

## 4. (20%) Cache

- 4.1 (2%) How many bits in total (including the tag bits and valid bits) are required for a direct-map cache with 16K bytes of data and 16-byte blocks, assuming a 32-bit address and one valid bit for each cache block?
- 4.2 (2%) Repeat the above problem for a two-way set-associative cache.

背面有題

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- 4.3 (2%) Repeat the above problem for a fully associative cache.
- 4.4 (4%) Compare the advantages and disadvantages of the above three different cache designs. Which one is usually used in the design of TLB (translation lookaside buffer)? Why?
- 4.5 (2%) The average memory access time (AMAT) per instruction can be expressed as  
$$\text{AMAT} = \text{time for a hit} + \text{miss rate} * \text{miss penalty}$$
  
Find the AMAT for a processor with a 1ns clock cycle time, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are the same and ignore other write stalls.
- 4.6 (4%) Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI (cycle per instruction) of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 36%.
- 4.7 (2%) Suppose that in 1000 memory references, there are 40 misses in the first-level cache and 20 misses in the second-level cache. Assume the miss penalty from L2 cache to memory is 200 clock cycles, the hit time of L2 cache is 10 clock cycles, and the hit time of L1 cache is 1 clock cycle. What is the average memory access time? Hint: average memory access time =  $L1\_hit\_time + L1\_miss\_rate * (L2\_hit\_time + L2\_local\_miss\_rate * L2\_miss\_penalty)$  where the  $L2\_local\_miss\_rate$  is the number of misses in L2 cache divided by the total number of memory accesses to L2 cache.
- 4.8 (2%) Continued with the previous problem, and assuming that there is 1.5 memory references per instruction, what are the average stall cycles per instructions? Hint: average memory stall per instruction =  $L1\_misses\_per\_instruction * L2\_hit\_time + L2\_misses\_per\_instruction * L2\_miss\_penalty$
5. (20%)
- 5.1 (5%) What is the advantage of single instruction multiple data (SIMD)? Compare the differences between SIMD in conventional CPU (Central Processing Units) and SIMD in GPU (Graphics Processing Units)
- 5.2 (5%) What is control hazard? Propose a method to improve the performance degradation due to control hazard.
- 5.3 (5%) What are the differences of spatial locality and temporal locality during execution of computation tasks in CPU? Give two programming techniques to explain the differences.
- 5.4 (5%) What is static multiple issue? What is dynamic multiple issue? Compare the differences.