

國立中山大學 105 學年度碩士暨碩士專班招生考試試題

科目名稱：計算機結構【資工系碩士班甲組、乙組】

題號：434001

※本科目依簡章規定「不可以」使用計算機(問答申論題)

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1. (20 %) SIMD, SIMT, VLIW, Superscalar, Superpipeline
 - 1.1 (4%) Explain the major features of single instruction multiple data (SIMD) processor. In other words, point out the major differences between SIMD CPU and conventional CPU. Give a practical example of SIMD instructions, CPU, or computer.
 - 1.2 (4%) Compare the differences of thread and process. Is context switching the change of threads or the change of process?
 - 1.3 (4%) Explain the major features of single instruction multiple threads (SIMT) processor. Give a practical example of SIMT computer.
 - 1.4 (4%) Explain the major features of very long instruction word (VLIW) processor. Which processor category does VLIW belong to, static multiple issue or dynamic multiple issue?
 - 1.5 (4%) What is a superscalar processor? What is a superpipeline processor?

2. (20%) Cache
 - 2.1 (4%) Give two methods to reduce cache miss rate.
 - 2.2 (4%) Give two methods to reduce cache hit time.
 - 2.3 (4%) Give two methods to reduce cache miss penalty.
 - 2.4 (4%) For the following Figure 1, explain the reason why the miss rate goes down as the block size increases to a certain level, and explain the reason why the miss rate goes up if the block size is too large relative to the cache size.

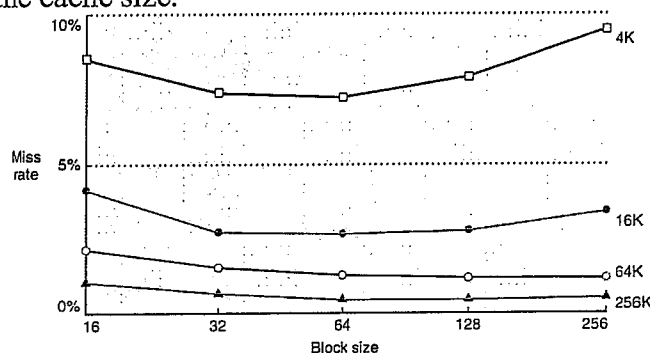


Figure 1.

- 2.5 (4%) Explain the differences of write-allocate and no-write-allocate during cache write miss.

3. (20%) The execution of an instruction can be divided into five parts: instruction fetch (IF), register read (RR), ALU operation (EX), data access (MEM), and register write (RW). The following Table 1 shows the execution time of each part for several types of instructions, assuming that the multiplexors, and control unit have no delay.

Table 1.

Instruction class	Instruction fetch	Register read	ALU operation	Data access	Register write
Load word (lw)	200 ps	100 ps	200 ps	200 ps	100 ps
Store word (sw)	200 ps	100 ps	200 ps	200 ps	
R-format (add, sub, AND, OR, sllt)	200 ps	100 ps	200 ps		100 ps
Branch (beq)	200 ps	100 ps	200 ps		

If instructions are to be executed in a pipelined CPU with five pipeline stages, IF, RR, EX, MEM, RW where the pipeline stages execute the corresponding operations mentioned above.

- 3.1 (4%) What is the cycle time of the pipelined CPU? What is the maximum working frequency?
- 3.2 (4%) What is the latency of executing the load-word instruction (lw) in the pipelined CPU?
- 3.3 (4%) What is the latency of executing the add instruction (add) in the pipelined CPU?
- 3.4 (4%) What is the maximum throughput of the pipelined CPU?
- 3.5 (4%) Propose a design method to increase the throughput performance of the pipelined CPU.

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4. (20%) Memory Hierarchy

The following Figure 2 shows the process of going from a virtual address to a data item in cache. Answer the following questions based on this figure.

4.1 (4%) What is the purpose of the translation lookaside buffer (TLB)?

4.2 (4%) Is the TLB direct mapped, set associative, or full associative? Is the data cache, direct mapped, set associative, or fully associative?

4.3 (4%) What is the page size? What is the block size of the data cache?

4.4 (4%) What is the size of the data cache (excluding the tags)? What is the maximum size of physical memory supported in this memory system?

4.5 (4%) Is the cache virtually addressed or a physically addressed?

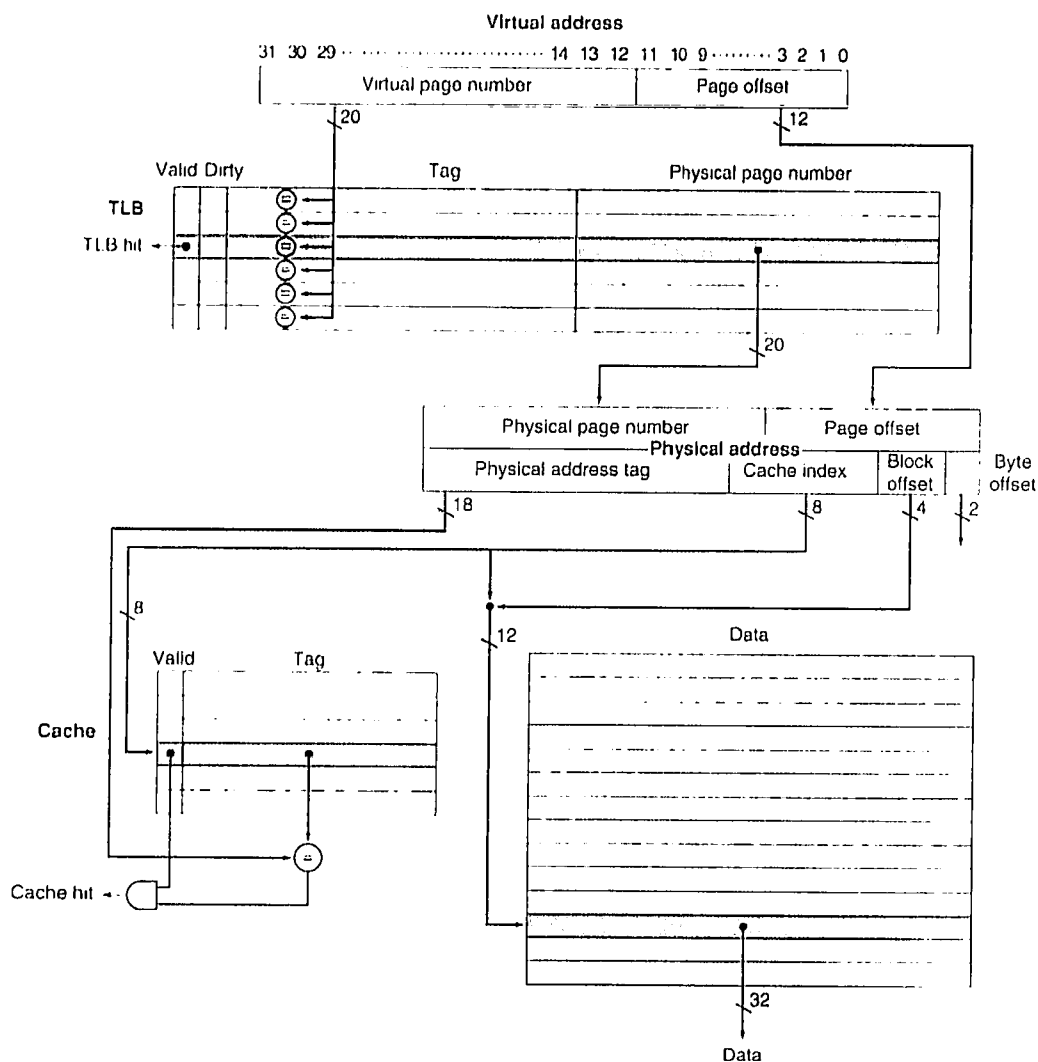


Figure 2.

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5. (20%) Answer the following questions.

5.1 (4%) What are the differences of arithmetic mean and geometric mean? Is geometric mean or arithmetic mean used by SPECINT2006 to summarize the speed measurements for several benchmark programs?

5.2 The following Figure 3 shows the growth in processor performance since mid-1980s. Answer the following questions.

5.2.1 (4%) Is the vertical axis of Figure 3 linear scale or log-scale? What is the growth rate, linear or exponential, if it is a straight line in a particular time interval in Figure 3?

5.2.2 (4%) Give two possible reasons for the large performance growth rate from 1986 to 2002.

5.2.3 (4%) Give two possible reasons to explain why the growth rate slows down after 2002.

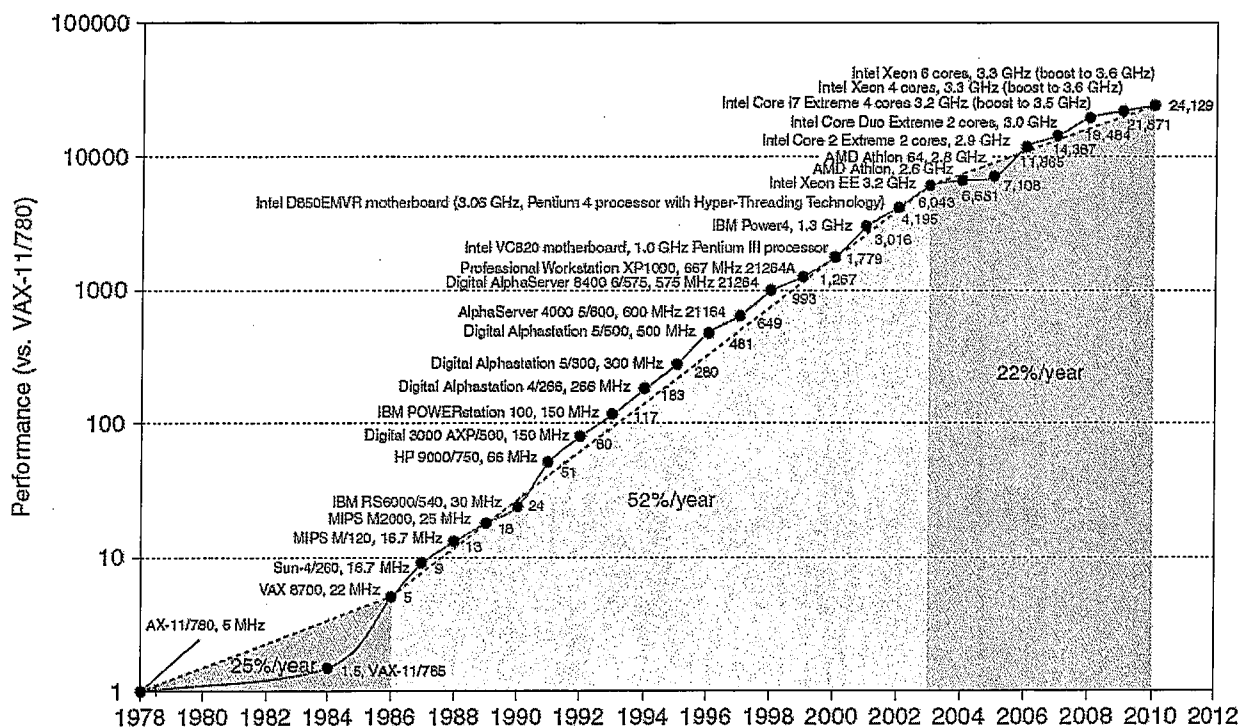


Figure 3.

5.3 (4%) Give two design methods to increase the performance of executing conditional branch instructions.