

國立中山大學 103 學年度碩士暨碩士專班招生考試試題

科目名稱：計算機結構【資工系碩士班甲組、乙組】

題號：434001

※本科目依簡章規定「不可以」使用計算機

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1. (12%) Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.

		Clock Rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
(a)	P1	2.5 GHz	1	2	3	3
	P2	3 GHz	2	2	2	2
(b)	P1	2.5 GHz	2	1.5	2	1
	P2	3 GHz	1	2	1	1

- (a) Given a program with 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster? (7%)
- (b) What is the global CPI for each implementation? (5%)
2. (14%)
- (a) $(520)_{10} = (\quad)_8 = (\quad)_{16}$. (4%)
- (b) Convert the decimal number -320 into signed 10-bit binary number in the 2's complement representation. (2%)
- (c) Assume that signed numbers are stored in 10-bit words in 2's complement representation. What is the result of $(256)_{10} + (257)_{10}$? (4%)
- (d) Show the IEEE 754 binary representation of the number $(-0.75)_{10}$ in single precision. (4%)
3. True or False Questions: (12%)
- (2%) (a) A multi-core processor consists of multiple chips, each containing a processor.
- (2%) (b) A server is a computer composed of hundreds to thousands of processors and terabytes of memory.
- (2%) (c) Access time to random access memory (RAM) is longer than access time to hard disk.
- (2%) (d) Assembly language consists of commands that processors understand.
- (2%) (e) The application software is software/programs developed by the users.
- (2%) (f) NaN in IEEE 754 can be the result of dividing 0 by 0 (0/0).
4. (10%)
- Consider the segment of MIPS assembler code below.
- ```
lw $v1, 0($a0)
add $v2, $v2, $v1
sw $v2, 0($a1)
addi $a0, $a0, 1
```
- (a) How many times is instruction memory accessed? How many times is data memory accessed? (Count only accesses to memory, not registers.) (6%, 3% each for two subproblems)
- (b) What are the addressing modes used in the four instructions? (4%)

5. (14%)

The latency of a block of digital logic is the time needed to do the work in the block. Assume that logic blocks needed to implement a processor's datapath have the following latencies:

| I-Mem | Add  | Mux  | ALU  | Reg's | D-Mem | Sign-Extend | Shift-Left-2 |
|-------|------|------|------|-------|-------|-------------|--------------|
| 200ps | 70ps | 20ps | 90ps | 90ps  | 250ps | 15ps        | 10ps         |

Consider the following datapath using the above logic blocks.

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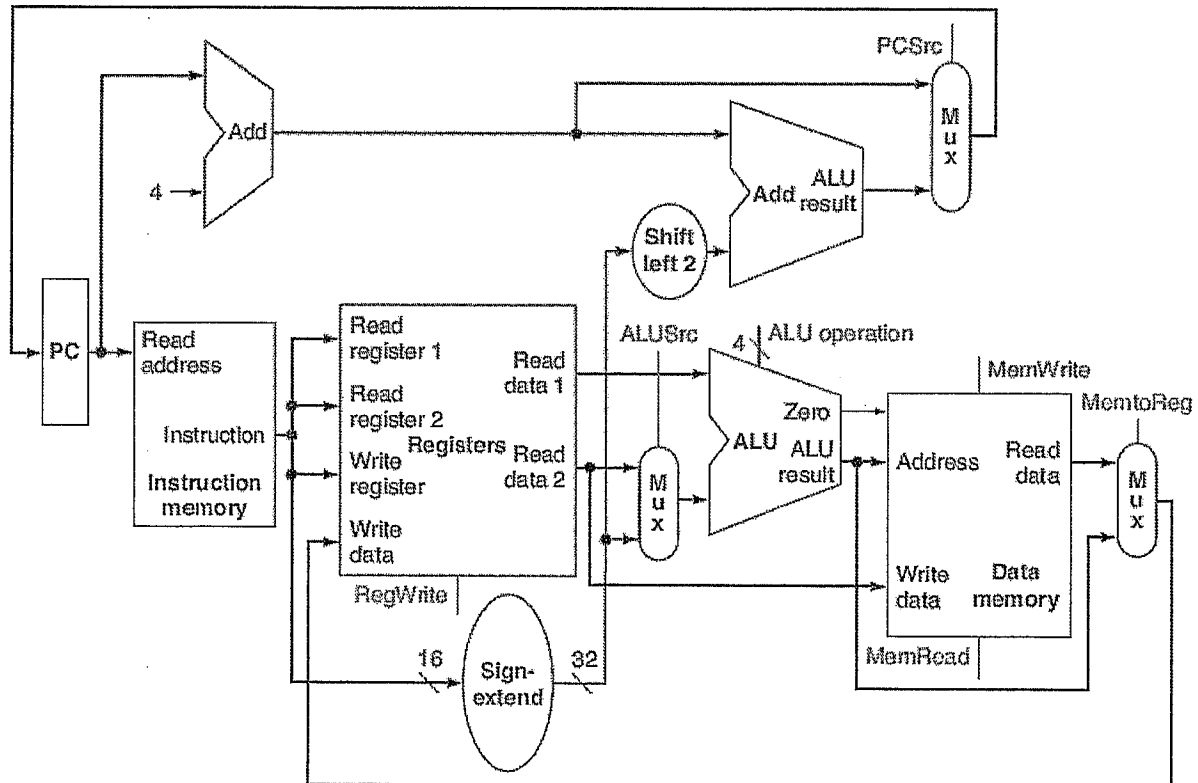
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- (a) What is the clock cycle time if the only types of instructions we need to support are ALU instructions (ADD, AND, etc.)? (5%)
  - (b) What is the clock cycle time if we only have to support LW (load word) instructions? (5%)
  - (c) What is the clock cycle time if we must support ALU, branch, load/store instructions? (4%)
- (Hint: You need to find the overall latencies of the blocks in the longest path required to execute an instruction.)

6. (10%)

Let the above datapath be implemented with pipelining. Assume that individual stages of the datapath (Instruction Fetch, Instruction Decode, Execution, Memory access, Write Back) have the following latencies:

| IF    | ID    | EXE   | MEM   | WB    |
|-------|-------|-------|-------|-------|
| 250ps | 350ps | 150ps | 300ps | 200ps |

- (a) What is the clock cycle time in a pipelined and non-pipelined processor? (5%)
- (b) What is the total latency of an LW instruction in a pipelined and non-pipelined processor? (5%)

7. (8%)

Assume that you are using a standard 5-stage pipelined processor (as shown in Problem 6) to execute the following MIPS instructions:

lw \$1,40(\$6)

add \$6,\$2,\$2

sw \$6,\$50(\$1)

- (a) Indicate dependences and their type. (4%)
- (b) Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them. (4%)

8. (12%) Cache system

- (a) Consider a direct-mapped cache with 16KB of data and 16-byte blocks, assuming a 32-bit

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address. What is the length of the tag field? How many total bits are required, assuming a valid bit is used? (6%)

- (b) Assume an instruction cache miss rate for gcc of 2% and a data cache miss rate of 4%. If a machine has a CPI of 2 without any memory stalls and the miss penalty is 40 cycles for all misses, determine how much faster a machine would run with a perfect cache that never missed. Assume 36% of instructions are loads/stores. (6%)

9. (8%) Briefly explain the following terms:

- (a) Page fault (4%)
- (b) Direct memory access (DMA) (4%)